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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/673,678	JACOB ET AL.	
	Examiner	Art Unit	
	Ryan P. Fiegle	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Claims 3, 9 and 14 refer to a memory on the first processing node (control node) that stores operating system code (executable code in claim 3, defined as operating system code in claim 5). Nowhere within the specification does it say that this memory contains operating system code. The specification simply states several times that the k-node executes the operating system code (Paragraphs 28, 38 and 74). Further the only mention of where executable code defining the functions (comprising the operating system code) is attained is in paragraph 35, which says that it is received from the Internet or a memory.

For the purposes of this action, claim 3 has been reworded to state, "... stored in at least a ~~said first~~ memory." Claim 9 has been reworded to state, "... a memory ~~for storing operating system executable code~~ ..." Claim 14 has been reworded to state, "... a memory ~~for storing operating system executable code~~ ..."

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 7-9, 14, 16, 17 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Master et al. (US PGPub 2002/0138716).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

3. As per claim 1:

Master et al. teach an integrated circuit comprising:

a plurality of computational elements including a plurality of arithmetic nodes, a plurality of bit-manipulation nodes, a plurality of finite state machine nodes, and a plurality of input/output nodes (¶45);

a first and a second processing node each having a core processor based on a common architecture (¶12; ¶47; ¶28) (Paragraph 12 shows that they have common architectures. Paragraph 47 shows that each matrix has a core. Paragraph 28 that either the KARC or MARC can constitute a first node.);

a first memory associated with said first processing node; a second memory associated with said second processing node (¶44; Figure 4) (Paragraph 44 shows that

each mode has local memory. Figure 4 shows that the memory is associated with the core of the node.);

a first node wrapper for coupling said core processor of said first processing node to said first memory and to said computational elements (¶29; ¶45; ¶47; Figure 3, data interconnect network);

a second node wrapper for coupling said core processor of said second processing node to said second memory and to said computational elements (¶25; ¶29; ¶45; ¶47) (Paragraph 25 shows that the MARC and KARC are made of the same matrices as the first processing node, and therefore will be set up the same way.); and

means for interconnecting said computational elements and said first and second processing nodes to define a selected task to achieve a desired functionality (¶29; ¶40).

4. As per claim 2:

The integrated circuit of claim 1 further comprising means for temporally adapting said second node and said computational elements to perform a selected function (¶40).

5. As per claim 3:

The integrated circuit of claim 2 wherein said temporal means further comprises executable code defining said selected function stored in at least a memory (¶40).

6. As per claim 7:

The integrated circuit of claim 1 wherein said computational elements include a plurality of arithmetic nodes, a plurality of bit-manipulation nodes and a plurality of finite state machine nodes (¶45).

7. As per claim 8:

The integrated circuit of claim 1 further comprises a plurality of said second processing nodes each of which is coupled to said first processing node and computational elements by said interconnecting means (Figure 1).

8. As per claim 9:

An adaptive computing engine comprising:

a controller node having:

a core processor for executing operating system code (¶40; ¶47);

a memory (¶44);

means for transferring operating system executable code and data from said memory to said core processor (¶29);

a plurality of computational elements adapted to perform a selected function at least one of said computational elements having:

a RISC processor for executing code (¶28);

a memory for storing executable code (¶44);

means for transferring executable code and data from said memory to said RISC processor (¶29); and

a temporal interconnecting matrix coupling said controller node to said plurality of computational elements to perform a user selected function (Figure 1).

9. As per claim 14:

An adaptive computing engine having a plurality of computational elements and a temporal interconnecting matrix for connecting said computational elements, said adaptive computing engine comprising:

a controller node for adapting said computational elements in response to perform a selected function (¶40), said controller node having:

a core processor for executing operating system code (¶47);

a memory (¶44);

means for transferring operating system executable code and data from said memory to said core processor (¶29);

a set of registers associated with said core processor (¶47);

a node wrapper, coupled to said core processor, for receiving an input stream from an external source, said input stream having configuration information and executable code and passing said information to said core processor (¶29); and

means for accessing said set of registers (¶29);

an interrupt controller for detecting interrupt conditions from said node wrapper and internally (¶29) (The network interconnect handles control and I/O signals which cause interrupts; an interrupt controller is inherent since the interrupts need to be handled).

10. As per claim 16:

The adaptive computing engine of claim 14 further comprising means for handling node-to-node communication (¶29).

11. As per claim 17:

The adaptive computing engine of claim 14 further comprising executable code for controlling the temporal adaptation of said computation elements in response to configuration information (¶40).

12. As per claim 22:

The adaptive computing engine of claim 14 further comprising means for minimizing power consumption (Abstract).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 4-6 and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Master et al. (US Patent 2002/0138716) as applied to claims 3 and 17 above in view of Fallside et al. (US Patent 6,326,806).

15. Master et al. teach claims 3 and 17 for the reasons stated above.

16. As per claim 4:

Master et al. does not teach the integrated circuit of claim 3 wherein said executable code is downloaded from the Internet by said first processing node in which Fallside et al. do (Fallside et al.: column 1, lines 63-67; column 2, lines 1-9).

Fallside et al. comment that FPGA systems are at a disadvantage because reconfiguring an FPGA requires special hardware, while other systems can be

upgraded from the Internet. Therefore, it would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention that applying Fallside et al. to Master et al. would provide the advantage of easier reconfiguration by using the Internet.

17. As per claim 5:

The integrated circuit of claim 4 wherein said executable code comprises operating system code (Master et al.: ¶41).

18. As per claim 6:

The integrated circuit of claim 5 wherein said first processing node initiates the temporal adaptation of said computational elements and said second processing node to perform said selected function (Master et al.: ¶41).

19. As per claim 18:

The adaptive computing engine of claim 17 further comprising means for controlling the initiation of operation of said computational element upon reset or power on (Fallside et al.: column 2, lines 2-9) (Motivation for applying Fallside to Master is provided above).

20. As per claim 19:

The adaptive computing engine of claim 18 further comprising:

a programmable scalar node having:

a core processor for executing instructions (Master et al.: ¶47);

an instruction memory for storing said instructions (Master et al.: ¶44) (The local memory can hold "processing function" data);

a data memory (Master et al.: ¶44);

means for transferring instructions from instructions memory to said core processor and for transferring data to said core processor from said data memory (Master et al.: ¶29);

a set of registers associated with said core processor (Master et al.: ¶47);

a node wrapper, coupled to said core processor, for receiving an input stream from controller node, said input stream having configuration information (Master et al.: ¶29); and

means for accessing said set of registers (Master et al.: ¶29); an interrupt controller for detecting internal interrupt conditions (Master et al.: ¶29) (The network interconnect handles control and I/O signals which cause interrupts; an interrupt controller is inherent since the interrupts need to be handled).

21. As per claim 20:

The adaptive computing engine of claim 19 further comprising:

a data cache; and

an instruction cache (Official Notice) (Though Masters does not disclose an instruction cache and a data cache, such are very well known in the art as well as their known advantages, and it is obvious to see why Master et al. would have motivation to add them).

22. As per claim 21:

The adaptive computing engine of claim 20 further comprising a memory arbitration unit for managing access to said data memory and said instruction memory (Master et al.: ¶29) (The interconnection network takes care of memory accesses).

23. Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Master et al. (US Patent 2002/0138716) as applied to claim 9 above in view of Trimberger et al. (US Patent 5,646,545).

24. Master et al. teach claim 9 for the reasons stated above.

25. As per claim 10:

Master et al. do not teach the adaptive computing engine of claim 9 wherein said controller node further comprises a configuration register, said configuration register containing a bit for determining whether said controller node functions as a controller or as a RISC processor.

Though Master states that the controller can be a FSM or a RISC processor, he does not disclose changing between these two configurations.

Trimberger discloses a state register, which keeps track which configuration a FPGA is in and blocks other memory cells containing other configurations while in that state (Trimberger et al.: Abstract).

Trimberger states that prior ways of reconfiguring FPGAs is time consuming and that his method will save time in reconfiguring (Trimberger et al.: column 1, lines 50-61).

Therefore, it would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention that applying Trimberger et al. to Master et al. would make the reconfiguration of the controller faster.

26. As per claim 11:

The adaptive computing engine of claim 10 wherein said configuration register bit protects a portion of memory from access by said computational elements when set (Trimberger et al.: Abstract).

27. As per claim 12:

The adaptive computing engine of claim 10 further comprising a protected portion of memory accessible only to said controller node (Master et al.: ¶44).

28. As per claim 13:

The adaptive computing engine of claim 9 wherein said controller node further comprises:

a node wrapper having:

a data distributor for receiving an input stream from an external source, said input stream having configuration information and executable code (Master et al.: ¶29, ¶40, ¶41);

a hardware task manager for receiving configuration information from said data distributor (Master et al.: ¶41);

a DMA engine for receiving data and executable code from said data distributor (Master et al.: ¶29; ¶40);

a controller for providing said node wrapper access a set of registers associated with said core processor (Master et al.: ¶47);

an interrupt controller for detecting interrupt conditions from said node wrapper and internally (Master et al.: ¶29) (The network interconnect handles control and I/O

signals which cause interrupts; an interrupt controller is inherent since the interrupts need to be handled); and

a JTAG port associated with a debug register for debugging erroneous operation of said controller node (Official Notice) (JTAG and its advantages are well known in the art, and it is obvious to see why Master et al. would have motivation to add it.).

29. Claim 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Master et al. (US Patent 2002/0138716) as applied to claim 14 above.

30. Master et al. teach claim 14 for the reasons stated above.

31. As per claim 15:

Master et al. do not teach the adaptive computing engine of claim 14 further comprising means for accessing said core processor and said memory to debug error conditions.

This would entail a JTAG controller, which is well known in the art along with its many known advantages, and it is obvious to see why Master et al. would have motivation to add it (Official Notice).

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